IN THE CLAIMS

Please amend and consider the claims as follows:

1. (Currently Amended) An apparatus, comprising:

a unitary capacitor having a bottom surface, a top surface, and an aperture in a central portion thereof extending from the top surface to the bottom surface; and

wherein the bottom surface is provided with electrical connections adapted to be connected to a substrate, and

wherein the unitary capacitor is configured such that when the unitary capacitor is disposed on a top surface of a package substrate, a surface area of an uncovered peripheral portion of the top surface of the package substrate is no greater than 21% of a total surface area of the top surface of the package substrate, the uncovered peripheral portion defined as a surface area of the top surface of the package substrate between an outside perimeter of the unitary capacitor and a perimeter of the package substrate.

2. (Previously Presented) The apparatus of Claim 1, wherein the aperture is rectangular.

3. (Previously Presented) The apparatus of Claim 1, wherein the unitary capacitor comprises a layer of an electrically conductive material and a layer of a dielectric material.

4. (Previously Presented) The apparatus of Claim 3, wherein a housing of the unitary capacitor is made from a plastic material.

5. (Previously Presented) The apparatus of Claim 1, wherein said electrical connections provided on the bottom surface comprise a ball grid array.

6. (Previously Presented) The apparatus of Claim 1, wherein the unitary capacitor comprises co-fired ceramic.

7. (Previously Presented) The apparatus of Claim 1, wherein the aperture is configured to fit over a semiconductor die, and wherein said electrical connections are configured for connection to a package substrate on which the semiconductor die is mounted.

8. (Currently Amended) A semiconductor package assembly, comprising:

a semiconductor die mounted on a portion of a top surface of a package substrate; and

a unitary windowframe capacitor having an aperture formed therein, and mounted on the top surface of the package substrate surrounding the semiconductor die, ~~wherein the unitary windowframe capacitor is arranged to substantially cover an available area of the top surface of the package substrate~~

wherein a surface area of an uncovered peripheral portion of the top surface of the

package substrate is no greater than 21% of a total surface area of the top surface of the package substrate, the uncovered peripheral portion defined as a surface area of the top surface of the package substrate between an outside perimeter of the unitary windowframe capacitor and a perimeter of the package substrate.

9. (Original) The semiconductor package assembly of Claim 8, further comprising an electronic component mounted on a top surface of the windowframe capacitor.

10. (Original) The semiconductor package assembly of Claim 8, further comprising a second windowframe capacitor mounted on a top surface of the first windowframe capacitor.

11. (Original) The semiconductor package assembly of Claim 8, wherein the aperture is rectangular.

12. (Original) The semiconductor package assembly of Claim 8, wherein the windowframe capacitor comprises a housing.

13. (Original) The semiconductor package assembly of Claim 12, wherein the windowframe capacitor comprises a capacitive material disposed within the housing.

14. (Original) The semiconductor package assembly of Claim 13, wherein the capacitive material comprises a layer of an electrically conductive material and a layer of a dielectric material.

15. (Original) The semiconductor package assembly of Claim 14, wherein the housing is made of a plastic material.

16. (Original) The semiconductor package assembly of Claim 13, wherein the capacitive material and the housing comprise a co-fired ceramic.

17. (Original) The semiconductor package assembly of Claim 8, wherein the windowframe capacitor is mounted on the package substrate via a ball grid array.

18. (Canceled)